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A REVIEW ON INTEGRATION OF SPIN RAM IN FPGA CIRCUITS

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ABSTRACT
In this paper, we propose a new non-volatile FPGA circuit based on Spin-RAM (or Spin Transfer Torque Magnetisation Switching RAM or STT RAM) technology, new generation of MRAM (Magnetic RAM). This Spin-RAM based FPGA circuit could process securely the information in low power dissipation and high speed, meanwhile all the data processed are stored permanently in the distributed Spin-RAM memory. The non-volatility of Spin-RAM allows the dynamical configuration of FPGA circuits and the start-up time of circuit can be decreased up to some hundred pico-seconds. In this non-volatile FPGA design, the circuit die area will not be enlarged as compared with the conventional FPGA

Keywords: STT-RAM or Spin RAM, FPGA, CLB, MRAM and MTJ.

I. INTRODUCTION

CMOS is currently the dominating technology for logic circuits, but is quickly approaching its scaling limits due to increased problems with power dissipation at scaled technology nodes. The increase in power dissipation results from the increase in static leakage (standby) power, as well as from the increase in density as the device size is scaled down. The integration of a fast, energy efficient non-volatile memory technology with CMOS can help alleviate this problem [8]. The conventional approach has been to use SRAM for caches, DRAM for main memory and rotating disks, Flash memory for storage. Each of these technologies has scalability limitations with regard to power consumption, performance and speed or reliability. Hence there comes an alternative approach to use a universal memory. It is to use a single universal memory that embodies all ideal properties of each layer having high performance, high density, high endurance, low power consumption and storage class non-volatility. Spin transfer torque RAM (STT-RAM) built using Magnetic Tunnel Junction (MTJ) is a promising "Universal Memory" candidate [5].

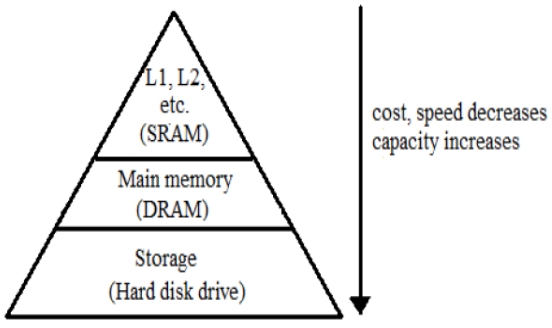

Figure 1: Schematic Representation of Memory Hierarchy

Most FPGA circuits use SRAM based configuration and Flip-Flop as internal memory; but as the SRAM is volatile both the configuration and the information stored in their internal registers are lost when the power is turned down. The configuration is then stored in an external PROM and downloaded

in the FPGA at start-up. Internal Flash technology is sometime used to replace the external memory, however its slow reprogramming and its limited number of writing cycles (up to 106) prevent its application to replace the SRAM based internal registers, which work at very high frequency. High writing and reading speed makes STT-RAM (Spin Transfer Torque Magnetization RAM) technology as one of the best solutions to bring a complete non-volatility to FPGA circuits while keeping low power dissipation [1].

II. SPIN TRANSFER TORQUE (STT) RAM

The ability to manipulate spin degree of freedom of conduction electron, in addition to charge, inspired an exciting new field "Spintronics".

STT-RAM has properties that make it a viable universal memory, it requires careful tuning to meet the requirements and constraints for each layer of the memory hierarchy. STT-RAM (Spin Transfer Torque RAM) has the advantages of non-volatility, theoretically unlimited endurance, fast, high density and low read and write energy equipment [4].One of the motivations in developing the STT based device is to reduce the high switching current needed in MRAM. Therefore, the STT effect is closely related with the field of memory. Since, the STT RAM has similar working principles as MRAM, all the applications of MRAM can be equally well catered using STT-RAM, but with higher density (translates to lower cost).

An STT-RAM cell consists of a Magnetic Tunnel Junction (MTJ) combined with an access transistor. The MTJ, which is the storage element, has an oxide layer sandwiched between two ferromagnetic (FM) layers. A MTJ behaves as a resistor with two resistance characteristics (high and low) depending on the magnetization direction in the two ferromagnetic layers. A MTJ presents a low (respectively high) resistance when the spin transport is in the same (resp. opposite) direction in two ferromagnetic layers and high resistance when the direction of spin is opposite.

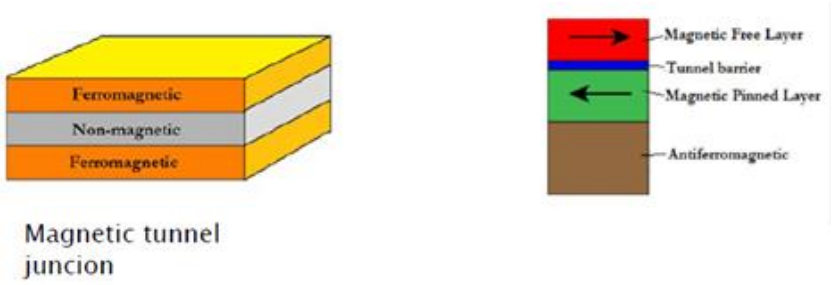

Figure 2: Magnetic Tunnel Junctions

The Tunnelling magnetic resistance (TMR) can be calculated by –

$$\text{TMR}=\frac{\Delta R}{R\uparrow\uparrow}=\frac{R\uparrow\downarrow-R\uparrow\uparrow}{R\uparrow\uparrow}$$

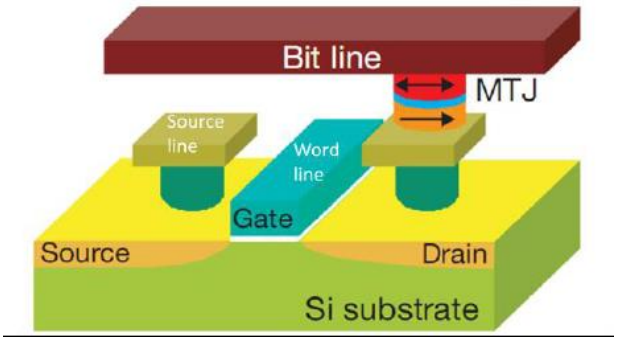

Figure 3: Basic structure of STT RAM memory cell

The first and most likely application for STT-RAM would be as embedded memory. Secondly, STT-RAM is suitable fast and continuous updates condition. This includes micro-controllers and robotics with data feedback in factory, printer system that handle large amount of users; and large data communication systems. Thirdly, STT-RAM can be used in high reliability conditions such as health care electronics, power management system and sever storage [4].

III. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

Field programmable gate arrays (FPGA) provides the next step in the programmable logic device (PLD) hierarchy. A Field programmable gate array is an integrated circuit designed to be configured by a customer or designer after manufacturing hence "Field Programmable". A Field programmable gate array (FPGA) is a VLSI circuit that can be programmed at the user's location FPGAs contain an array of programmable logic blocks and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together like many logic gates that can be inter-wired in different configurations. Logic bocks that can be configured to perform complex combinational functions or merely simple logic gates like AND and XOR. In most FPGAs logic blocks include memory elements which may be simple flip flops or more complete blocks of memory [6].

A typical FPGA consists of a millions of a logic blocks surrounded by a programmable input and output blocks and connected together via programmable connections. There is a wide variety of an internal connection within this group of devices [7]. The performance of each type of device depends on the circuit contained in its logic blocks and the efficiency of its programmed interconnections.

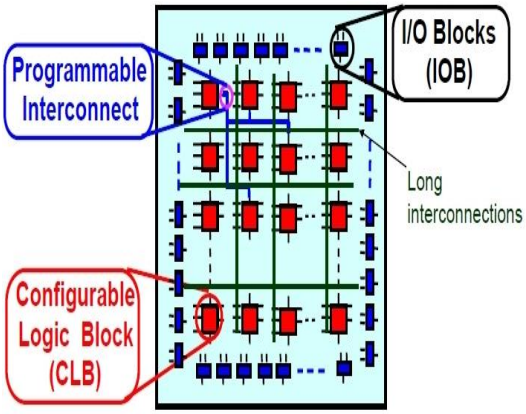

Figure 4: Structure of FPGA

Two basic FPGA architecture are offered by the product lines of two companies: Xilinx and the Actel. Both approaches have cells and modules that can be configured by the end user. Both require a switching matrix to interconnect the cells or modules. The Configurable Logic Block (CLB) resources can be used as desired and interconnected with other CLBs to form the completed design [7]. Xilinx uses an external memory to store the switch matrix configuration dat. By placing the interconnect information in a memory (EPROM or RAM) changes are permitted. This means that device can be reprogrammed by simply changing the configuration memory data.

IV. INTEGRATION OF SPIN RAM IN FPGA CIRCUITS

One of the main motivations of developing the STT-RAM based device is to reduce the high switching current needed in MRAM. Therefore, the application of STT effect are closely related to the field of memory. Since, the STT-RAM has similar principles as MRAM, all the applications of MRAM would be well catered using STT-RAM, but with a higher current density (translates to lower cost). Despite the obvious application of becoming the only standalone memory to replace other existing technologies, the most likely application being the "Integration of STT-RAM with FPGA circuits".

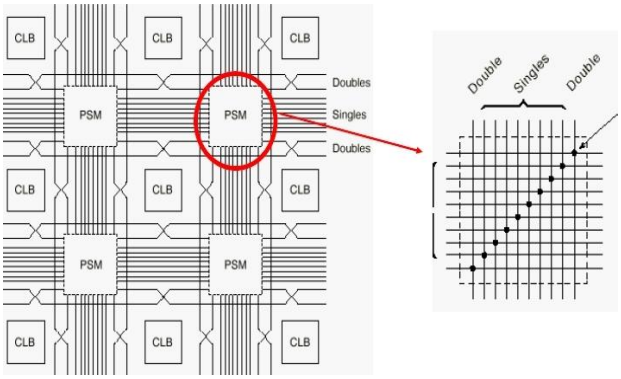

Figure 5: Interconnections in a FPGA

A switch matrix is used to interconnect the CLBs and I/O blocks as illustrated in Figure 4.1. Each switch block provides for direct interconnection between adjacent CLBs or I/O blocks. In addition, four vertical and two horizontal long lines permit interconnection between any CLB in the FPGA chip. The interconnection switch memorizes the connection routes between the logic elements.
In a conventional FPGA circuit, the interconnection includes 6 transistors and 6 SRAM which must be programmed at the circuit start-up. Due to non-volatility of the Spin-RAM, the FPGA circuit does not require the external flash ROM.

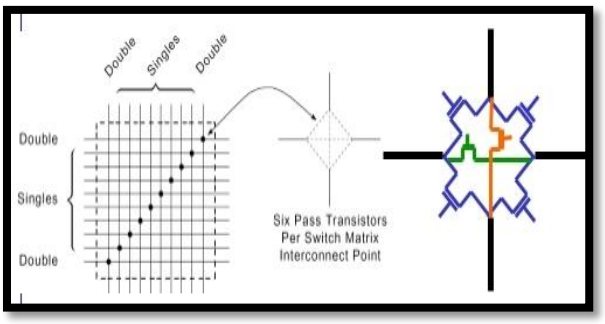

Figure 6: Programmable Switch Matrix

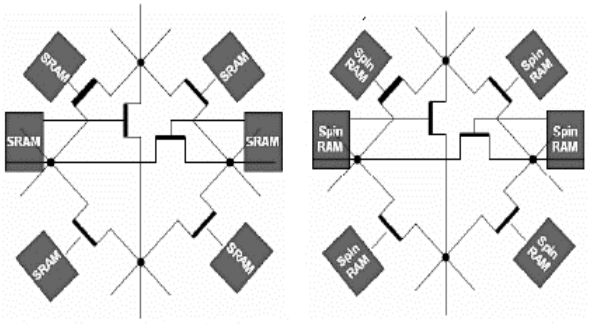

Figure 7: Interconnections based on SRAM and Spin-RAM

V. CONCLUSION

The intrinsic properties of spin-based systems make them advantageous as a prospective candidate for fast, dense and energy efficient non-volatile memory devices. STT-RAM, where a spin-polarized current is used to manipulate the magnetization state of an MTJ, has become one of the emerging candidates particularly for embedded memory, since it can be directly integrated with CMOS, matching or outperforming SRAM, DRAM or Flash in most respects.

Spin-RAM provides all the advantages of non-volatility, high speed, low power dissipation and high density, and this demonstrates that Spin-RAM technology is a very promising solution for the future FPGA. This Spin-RAM based FPGA features simultaneously non-volatility, high processing speed and low power dissipation. Multi-context configuration or dynamical re-configuration FPGA can be implemented easily and with small physical surface overhead, therefore it could be a technological choice in multi functions processing circuit, such as MP3 player or Mobile phones.
STT-MRAM based–FPGA logic circuits are presented in this article, which can perform runtime reconfiguration, multi-context configuration, and "instant-on" start-up with low power dissipation, small area, and at high speed. This non-volatile FPGA logic circuit has great potential to replace all the types of current FPGA circuits in the high-performance computing and those embedded in mobile equipment powered by the battery. They could be advantageously used in the field of aviation and space where the data hardness to radiation is one of the most important considerations.

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