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DESIGN AND IMPLEMENTATION OF ADIABATIC LATCH FOR LOW POWER EMBEDDED SYSTEMS

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ABSTRACT

With increasing complexity in today's world and new requirements of more computation power and more facilities on same chip. The requirement of low power circuits has become inevitable. The low power digital circuits are evolving as a principal factor in electronics now a days. For designing any digital circuit several parameters of design metrics are to be considered and it often happens while optimising one parameter one has to compromise other parameter of design metric for example area or no. of gates may be compromised to reduce power dissipation. This paper presents design and implementation of adiabatic latch. The latch serves as basic memory element and it can serve as basic building block for hierarchical memory designs. The proposed adiabatic latch which serves as a one bit memory element is designed. The technique used to design the latch is based on reducing power dissipation based on Efficient Charge Recovery Logic (ECRL).The proposed design approach reduces the power dissipation significantly. The adiabatic technique used for designing latch uses adiabatic power clock based supply instead of constant power supply so that the power dissipated can be restored by changing the direction of current. The work is implemented using PSPICE130-nmtechnology.

KEYWORDS: *Adiabatic, Efficient Charge Recovery Logic (ECRL)*

I. INTRODUCTION

With the increase in complexity and no. of functionalities on single chip minimizing power consumption has become one of the biggest design challenge in the field of VLSI. The optimization of power consumption is an important factor in any electronic device and system. Further, the mobile devices have stringent ever growing requirement of high performance, light weight, and long operation time, which requires more power consumption. The designers are forced to design circuits with reduced the power consumption of whereas keeping the same performance. The energy consumption of logic circuits designed using adiabatic techniques for reducing power consumption can be significantly reduced by returning charges to power supplies after the circuit operation. The energy loss in an adiabatic circuits consists of basically three types of losses i.e. adiabatic energy loss, non-adiabatic energy loss, and the basic energy loss due to the leakage current of MOSFETs. The adiabatic energy loss and the energy loss due to the leakage current are not avoidable. The adiabatic energy loss is proportional to the product of load capacitance and on – resistance of a MOSFET when we regard the MOSFET as a switch, and it is inversely proportional to the slope of the power supply waveform. The energy loss due to the leakage current is caused by the leakage current which is independent of the power supply slew rate. The non-adiabatic energy loss is caused by the threshold voltage which is needed to turn on the MOSFET switch. The reversible energy recovery logic focuses on reducing the non-adiabatic energy loss .Though the non-adiabatic energy loss is minimized using the efficient charge recovery logic; the large number of additional circuits for reversible computing degrades the energy efficiency at high frequency operation. The efficient charge recovery logic shows good energy consumption characteristics below 2MHz operation

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compared to the conventional CMOS logic. This kind of logic is suitable for the application where the operation frequency is not important and the energy consumption is of concern. In this paper, efficient charge recovery logic is used because the energy consumption is lower than the conventional CMOS

Efficient charge recovery logic (ECRL) is one of the adiabatic logic families and is useful for low energy systems. An energy-recovery method based on the adiabatic technique uses an AC power supply, and an efficient supply clock generator is essential for the design of a low power system using adiabatic circuits. Most of the previous works on adiabatic circuits have focused on building blocks such as adders and multipliers [6], [9] and their energy consumptions compared. The study on adiabatic circuits should not be limited to designing the building blocks. It is essential to design a complex system such as a microprocessor for the feasibility of adiabatic circuits. In order to implement a microprocessor, large macro blocks [10], random logic, and storage elements are necessary as building blocks. In particular, registers using adiabatic circuits have not yet been reported. In this paper an ECRL based adiabatic LATCH is proposed. The latch serves as 1-Bit storage element .It is an essential building block for designing memories, counters, registers and even microprocessors.

Rest of the paper is organized as follows, the conventional pulse triggered flip-flops are described in section II. The fundamental principles of adiabatic logic, different types of adiabatic logics, and the adiabatic latch designs based on ECRL adiabatic logic are described in section III. The simulation results for all the designs implemented using PSPICE simulator130-nm technology are discussed in section IV.

II. BACKGROUND

A latch is an asynchronous digital circuit that has two stable states – '0' and '1' that can be used to store state information.

2.1 SR Latch

One of the most fundamental latches is the SR latch, where S and R stand for Set and Reset. Figure 1 shows the logic diagram of an SR latch neither built using cross-coupled NOR gates. The stored bit is available at the output marked Q; its complement is available at output $\overline{Q}$.While the S and R inputs are both low, feedback maintains the two outputs in a constant state.

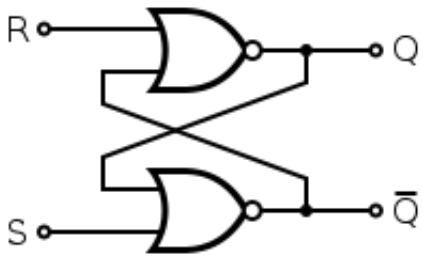

Figure 1A NOR-based SR Latch

When R = 1 and S = 0, output Q will go to 0 regardless of its value before R was set to 1, and that forces $\overline{Q}$ to 1 after a brief delay. Thus, R resets the output to 0. When R = 0 and S = 1, $\overline{Q}$ becomes 0 and Q becomes 1. Thus, input S sets the latch.

When R = S = 1, both Q and $\overline{Q}$ become 0, and are no longer complementary to each other. At this point, if both R and S are simultaneously switched to 0, both outputs will be forced to become 1, which in turn will try to force both outputs to become 0, and so on. If both NOR gates and the associated wires have the same delays, both outputs will oscillate indefinitely with a period of 2 gate delays. In reality, the two path delays will not be identical, forcing the latch to go to a stable state. Because the final output state will vary from one latch to another, the input combination R = S = 1 is not usually applied. It is up to the circuit designer to insure that this condition never appears.

An alternate model of the SR latch can be built with NAND gates, as shown in Figure 2. Set and reset now become active low signals, denoted S and R respectively. Otherwise, operation is identical to that

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of the SR latch. Historically, the NAND-based $\overline{SR}$ latch has been predominant, despite the notational inconvenience of active low inputs.

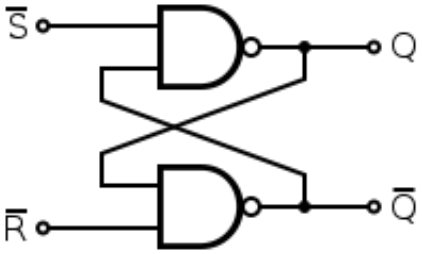

Figure 2A NAND-based S' R' Latch

III. ADIABATIC LOGIC

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source, as shown in Fig. 3. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage V_C is zero initially, the variation of the voltage as a function of time can be found as

$$V_C(t) = I_S.t/C. \quad (1)$$

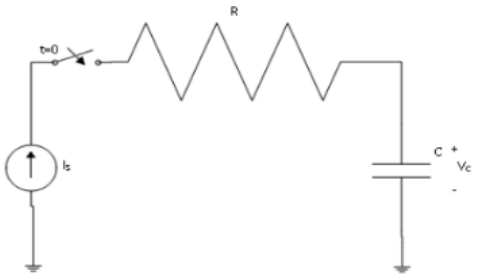

Figure 3 Capacitor charging through constant current source

Hence the charging current can be represented as a function of voltage V_C and time t.

$$I_S = C.V_C(t)/t \quad (2)$$

The amount of energy wasted or dissipated in resistor R from time t=0 to t=T can be found as

$$E_{diss} = R \int I_S^2 dt = RI_S^2 T \quad (3)$$

Combining (4) and (5), the dissipated energy during this charge-up transition can also be expressed as

$$E_{diss} = \{RC/T\}.CV_C^2(T) \quad (4)$$

From (4) we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies. The additional hardware overhead associated with these specific power supply circuits is one of the design trade-off. Practical supplies can be constructed by using resonant inductor circuits. But the use of inductors should be limited from integrated circuit point because of so many factors like chip integration, accuracy, efficiency etc.

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An alternative to using pure voltage ramps is to use stepwise supply voltage waveforms, where the output voltage of the power supply is increased and decreased in small increments during charging and discharging. Since the energy dissipation depends on the average voltage drop across the resistor by using smaller voltage steps the dissipation can be reduced considerably. The total dissipated energy using conventional charging technique is shown as (5)

$$E_{tdiss} = (1/n)\, CV_{DD}^2/2 \quad (5)$$

Where n represents the number of steps used for charging up the end capacitor to voltage $V_{DD.}$
Now couple of observations can be made based on Equation (5efficient charge recovery logic) as follows:

(i) The energy dissipated for adiabatic circuits is smaller if the charging time T is larger than $2RC_{L.}$

(ii) Since, the dissipated energy is proportional to R thus reducing the on- Resistance of pMOS reduces the energy dissipation.

3.1 Adiabatic Logic Families

Several adiabatic or Energy recovery logic architectures have been proposed over the years. They are based on the similar principle, but the structure and complexity, differ by, number of operation clock, Single- Dual rail style, Charging and discharging path etc.

3.1.1Adiabatic Logic Families Classification

Partially adiabatic logic. They are classified as –
(i) Efficient charge recovery logic (ECRL)
(ii) Quasi Adiabatic Logic(QAL)
(iii) Positive feedback adiabatic logic (PFAL)
(iv) NMOS energy recovery logic
(v) True single phase adiabatic logic (TSEL)
Fully adiabatic logic. They are classified as-
(i) Pass transistor adiabatic logic (PAL)
(ii) 2 Phase adiabatic Static CMOS logic
(iii) Split rail charge recovery logic (SCRL)

3.2 Efficient Charge Recovery Logic (ECRL)

On the basis of energy consumption and the specifications the ECRL is selected for the design of proposed adiabatic latch. Efficient Charge Recovery Logic (ECRL) is a type of quasi adiabatic logic family as discussed in section 3.1.1 above. A typical ECRL based circuit is shown in Figure 4, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors M3 and M4.As shown in the figure 4 an AC power supply'V4'is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and complement of out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. Full output swing is obtained because of the cross-coupled PMOS transistors in both precharge and recovers phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches threshold energy can be recovered from the circuit.

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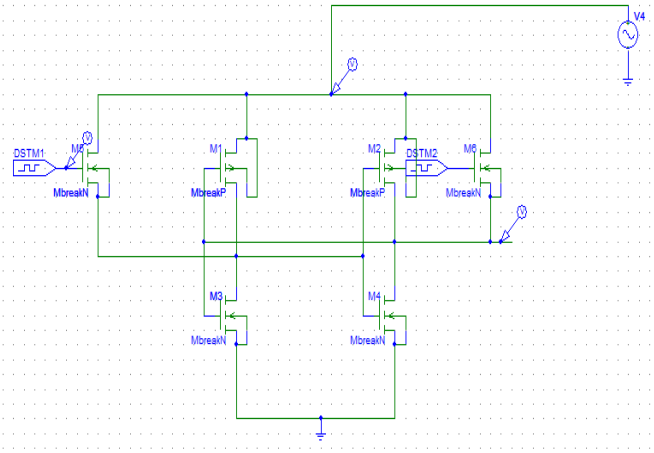

Figure 4A typical ECRL based Circuit

IV. DESIGN OF ECRL LATCH

The ECRL circuits are operated in pipelining style with the 4-phase supply clocks. When the output is directly connected to the input of the next stage (which is a combinational logic), only one phase is enough for a logic value to propagate. However, when the output of a gate is fed back to the input, the supply clocks should be in phase. A latch is one of the simplest cases which have a feedback path. The input signals propagate to the next stage in a single phase, and the input values are stored in4-phases (1-clock) safely.

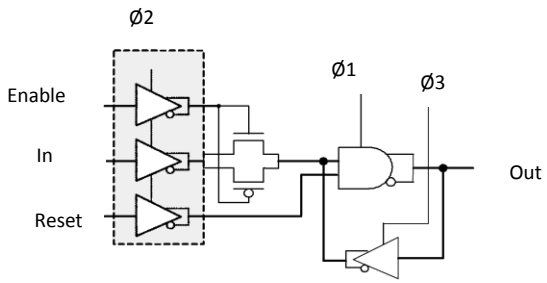

Figure 5 ECRL Latch [16]

Fig. 5 shows the basic structure of the proposed latch. The thick lines mean two complementary signals. The proposed circuit consists of four Buffers, a Pass transistor, and a nand gate. The circuit shown in figure 5 is implemented and a schematic for obtaining simulation results is drawn as shown in figure 6.The forward NAND gate A1 can be replaced by a simple inverter when the reset function is not needed. When a DC input is applied, the differential sinusoidal waveforms can be obtained by propagating through an additional buffer. The signals from switching transistors, M1 and M2, drive the next stage through the NAND gate powered by u1. The buffer I1 for storing the signal is powered by u3 and the phase is in accordance with A1.The buffer in the feedback path performs the 'precharge and evaluation' in the 'Recovery' phase of the NAND gate (A1) powered by u1. The waveform of the node 'node in' changes abruptly near the beginning and the end of the waveform, and oscillates according to the phase of u3. The NAND gate A1 could be replaced by an inverter when the 'reset' function is not necessary. Edge-triggered D flip-flops are commonly used in CMOS circuits because signals have glitches and the arrival times are not fixed. However, the signals of the ECRL circuits are synchronized to the supply clocks, and the arrival times of signals are almost the same so that the glitches are not produced. Therefore, the proposed simple latch is enough to perform storing operation correctly, and the gate count of the ECRL latch is very small compared with the conventional CMOS clocked logic flip-flop.

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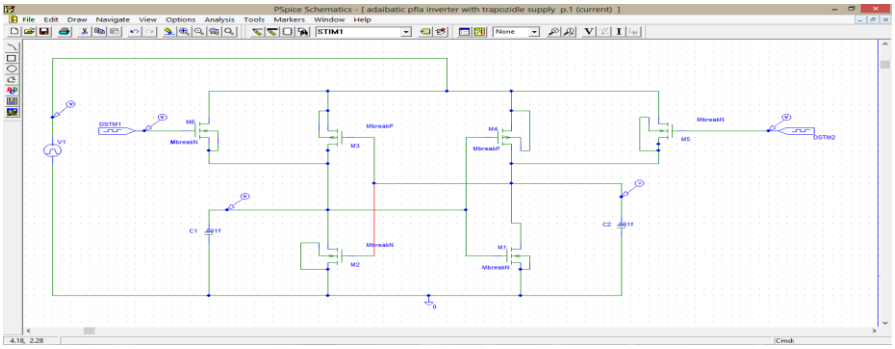

Figure 6 ECRL Latch Schematic

V. RESULTS AND DISCUSSION

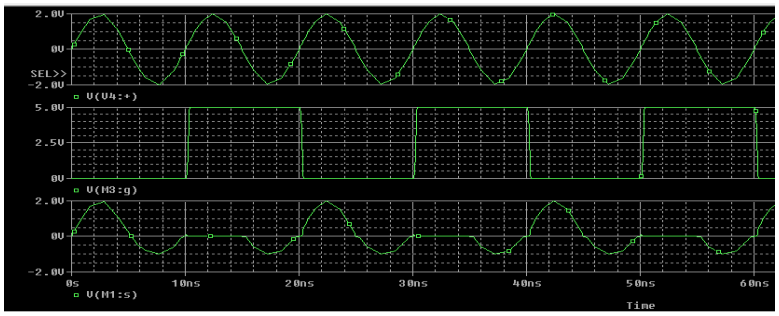

Figure 7 Output Waveform ECRL Latch

Fig. 7 shows the waveform of the latch operation in which the input value is stored according to the 'enable' signal. The gates driven by the output of the latch should be powered by u2, so that the 'precharge and evaluation' phase is accomplished during the 'Hold' phase of the latch. An input value applied to a latch propagates to the next stage in a single phase though 4-phases (1 clock) are necessary to store the input value to the latch safely because the input signal passes I1 and A1. A single ECRL latch was designed and implemented. For the ECRL latch adiabatic power supply clock generators is designed, and the energy consumption is analyzed. The energy consumption of proposed ECRL latch is significantly reduced as compared with CMOS latch of the same configuration taken from Chan Ho et. al. [16], and is expected to be 1/3 in practical circuits logic gates and memory elements. The energy consumption is not affected by the power supply clock frequency in the range of 100–400MHz.

VI. CONCLUSION

An ECRL latch used as a storage element in low power adiabatic circuit is designed implemented. The ECRL latch consists of a NAND gate, an inverter, and two MOSFET switches, and has the input signals of 'enable', 'reset', and 'input'. A single ECRL latch with a power supply clock generators are designed, and the energy consumption is analyzed. The energy consumption is about half of a CMOS SR latch and with the same configuration, and is expected to be 1/3 in practical circuits logic gates and memory elements. The energy consumption is not affected by the power supply clock frequency in the rangeof100–400MHz.The proposed ECRL latch can be a good choice of a low power storage element for the adiabatic microprocessors and embedded systems.

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